COOPER E. SHAW

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OBJECTIVE

Junior Computer Engineering student seeking an internship in computer architecture and VLSI physical design starting May '26

EDUCATION

GEORGIA INSTITUTE OF TECHNOLOGY, Atlanta GA ***Aug '23 – May '27***

Bachelor of Science in Computer Engineering GPA: Cumulative 3.48, Major 3.53

- *Threads*: Computing Hardware & Emerging Architectures and Systems & Architecture
- *Relevant Topics*: Pipelined Computer Architecture, Concurrency and Parallelism, Low Level Programming, Cache, RTL

EXPERIENCE

Silicon Jackets (Student-led Chip Design Club) | *Physical Design Team Member* ***Jan '25 – Current***

- Advocated for and created more extensive and accessible internal documentation to encourage new club member participation in the design process
- Completed Digital Design, Verification, and Physical Design team onboarding processes (See *Projects*)
- Participated in Physical Design Team Lead training process; projected to become PD Team Lead by Spring semester 2026

Tenovos | *Configuration Specialist, Contract* ***Aug '24 – Feb '25***

- Independently oversaw front-end of Tenovos Insights Reporting for 26 companies including Amazon, Mattel, and Lockheed Martin using SQL and AWS QuickSight
- Onboarded and trained a team of 3 full-time engineers to take over Configuration Specialist responsibilities
- Arranged and directed meetings with colleagues in engineering, operations, and product management teams to interpret, diagnose, and resolve issues reported by customers

Tenovos | *Instructional Design and Customer Success Intern* ***Jan '23 – Aug '24***

- Restructured and optimized outdated, highly technical platform documentation written by engineers into 20+ customer-facing user guides while adhering to structural and style precedents of existing platform documentation
- Led meetings teaching SQL, AWS Quicksight, and internal data management structures to full-time employees
- Spearheaded Tenovos API v1.5 endpoint functionality documentation project using Postman and Docusaurus

PROJECTS

Member Onboarding FSM ASIC Design Process, RTL to GDS | *Silicon Jackets* ***Jan '25 – March '25***

- Designed Greatest Common Divisor algorithm as a Mealy FSM in SystemVerilog
- Generated waveform in DVE to simulate FSM's behavior with a small sample of states and inputs
- Created testbench module and analyzed test case coverage in Synopsis Verdi, reaching 100% DUT coverage

Tenovos API v1.5 Documentation | *Tenovos* ***Jun '24 – Aug '25***

- Transformed technical outline detailing API endpoint functionality by generating test API calls to understand and correct inconsistent technical documentation written by Engineering team
- Interfaced with engineering team to clarify unexpected API behavior and translate technical explanations into accessible instructions with a consistent structure and formatting style

COURSEWORK

Architecture, Systems, Concurrency, and Energy in Computation | *Georgia Institute of Technology* ***May '25 – July '25***

- Debugged and completed partial RTL processor designs using SystemVerilog, iverilog, GTKwave, and ModelSim
- Simulated and analyzed various cache architectures, virtual memory, and OS thread scheduling in C

Digital Design Lab | *Georgia Institute of Technology* ***Jan '25 – May '25***

- Simulated SCOMP on an FPGA and implemented I/O hardware RTL to control DE-10 FPGA Board peripherals
- Implemented and simulated digital logic design using both block diagram schematics and VHDL using Intel Quartus
- Captured breadboard output using Signal Tap on Cyclone V FPGA board and verified results against simulated design
- Demonstrated proper equipment usage to peers and assisted in resolving software and hardware issues

GPU Programming for General Computing | *Georgia Institute of Technology* ***Jan '25 – May '25***

- Executed massively parallel CUDA programs on Georgia Tech's NVIDIA HGX H100 GPU cluster
- Learned about memory, cache, and microarchitecture of GPUs and similar highly parallel hardware accelerators

SKILLS AND INTERESTS

Technical: C, Verilog, TCL, Cadence EDA, RISC-V, Linux, Java, CUDA, SQL, Physical Design, Markdown, Quartus, STA
Soft Skills: Collaboration and Communication, Leadership, Workflow Optimization, Internal Documentation Creation
Professional: VLSI SoC and ASIC Physical Design, Emerging Architectures, FPGA Design Verification

CERTIFICATIONS

Cadence RTL-to-GDSII Flow v7.0